

Method and Apparatus for Wafer Scale Testing

ABSTRACT OF THE DISCLOSURE

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Methods and apparatus are provided for I/O pads of unsingulated integrated circuits, to be connected to electrical equipment. A translator plate is interposed between a wafer and tester. The translator plate includes a substrate having two major opposing surfaces, each surface having terminals disposed thereon, and
10 electrical pathways disposed through the substrate to provide for electrical continuity between at least one terminal on a first surface and at least one terminal on the second surface. The translator plate, when interposed between wafer and tester, makes electrical contact with one or more I/O pads of a plurality of integrated circuits on the wafer, providing an electrical pathway therethrough. An anisotropic
15 conductor is disposed between the wafer and the translator plate. A vibratory mechanism, oriented to provide substantially horizontal vibratory motion to the wafer, may be coupled to the wafer to assist disposing the translator plate and anisotropic conductor over the wafer.